REMARKS

Applicants are amending independent Claims 43, 49, 79, 85, 91, 97 103 and 109 to correct an informality in the claims. This amendment is not in response to a patentability rejection.

Applicants will now address both the Office Action and Examiner's interview summary.

In the Office Action of September 9, 2004, the Examiner had only one rejection of the claims. During the interview of November 18, 2004, the undersigned discussed the below listed arguments with the Examiner. The Examiner agreed that Applicants had overcome this rejection. The Examiner, however, issued a new rejection which is discussed *infra*. Applicants are repeating herewith their arguments in response to the rejection in the September 9, 2004 Office Action so as to overcome and remove that rejection.

September 9, 2004 Office Action

Claim Rejections - 35 USC §103

In the Office Action, the Examiner rejects Claims 43-54 and 79-112 under 35 USC §103(a) as being unpatentable over Balasubramanyam et al. in view of Hwang et al. This rejection is also respectfully traversed.

More specifically, the independent claims of the present application each recite that a bottom surface of the first conductive layer is in contact with the gate insulating film.

The Examiner contends that Balasubramanyam teaches a gate electrode 22, 24 adjacent to the gate oxide 18 with a gate insulating layer 20 interposed therebetween. The Examiner further contends that the gate electrode has a first conductive layer 22 comprising tungsten/nitride and a second conductive layer 24 comprising tungsten on the first conductive

layer. The Examiner then contends that the reference discloses the bottom surface of the first conductive layer 22 being in contact with the gate insulating layer 20 (and cites Fig. 8 of the reference in support thereof).

Applicants respectfully disagree. Balasubramanyam describes layer 20 as a doped polysilicon layer (see col. 5, lns. 34-36). Further, the doped polysilicon in the reference has a conductive property because it includes one conductivity type impurity. Furthermore, in Column 1, line 17 to 20 of Balasubramanyam, it is disclosed that the patterned N+ doped polysilicon and WSi_x layers comprise the gate conductor (GC) in the gate electrode stack. The reference is consistent throughout that the doped polysilicon is part of the gate electrode stack and is not the gate oxide or a gate insulating layer. See e.g. Balasubramanyam - col. 2, lns. 4-7 ("polysilicon gate electrode stack" distinguished from "gate oxide"), lns. 65-67 (distinguishing polysilicon layer from gate oxide); col. 3, lns. 23-34 (discussing a "polysilicon/gate oxide interface"); col. 6, lns. 25-42 (discussing the gate electrode stack as including layers 20, 22 and 24); claim 1 (defining the gate electrode as being above the gate oxide and comprising a doped polysilicon layer on the gate oxide layer). This is further evidence that the N+ doped polisilicon 20 is a conductive material which is part of the gate electrode stack and not the gate insulating layer.

Therefore, it is clear that layer 20 in Balasubramanyam is part of the electrode and not a gate insulating layer. It is well established that an electrode can be made of polysilicon. See e.g. "Microelectronics", Scientific American, p. 50 (1977).[1]

Hence, layer 20 is not the gate insulating layer, and Balasubramanyam does not disclose or suggest the claimed limitation that a bottom surface of the first conductive layer (which is

[1] See also 6th McGraw-Hill Electronics Dictionary (1997) definition of electrode which does not require the electrode to be made of metal). A copy of each of these cites is attached herewith.

defined in the claims as comprising nitride) is in contact with the gate insulating film.[2] Accordingly, it is respectfully requested that this rejection be withdrawn.

November 18, 2004 Interview

During the interview of November 18, 2004, the Examiner raised the possibility of a rejection of Claims 43-54 and 79-112 under 35 USC §103(a) as being unpatentable over Balasubramanyam et al. in view of Yamazaki et al. (US 6,362,027).[3] This rejection is also respectfully traversed.

More specifically, it is respectfully submitted that this rejection is not proper. The independent claims in the present application recite:

> said gate electrode comprises a first conductive layer comprising nitride and a second conductive layer comprising tungsten on said first conductive layer,
>
> wherein a bottom surface of said first conductive layer is in contact with the gate insulating film,

The Examiner appears to be proposing that it would have been obvious for one skilled in the art to take the structure in Balasubramanyam and insert therein a gate insulating film from Yamazaki '027. However, to arrive at the claimed invention (which has the first conductive layer of nitride in contact with the gate insulating layer), one would have to insert the gate insulating film of Yamazaki '027 between layers 20 and 24 in Balasubramanyam. However, there is simply no reason one skilled in the art would want to do this. Such an modification would require inserting a gate insulating layer between electrodes in a gate electrode stack. This makes no sense.

---

[2] Hwang is not cited for nor does it disclose or suggest this feature.

[3] It is not clear if this rejection is still in view of Hwang et al. However, for purposes of this amendment, whether that reference is cited or not is irrelevant.

Under MPEP §2143.01, there must be some motivation to combine references. References cannot be combined if there is no motivation to combine the references.

It is respectfully submitted that no such motivation exists herein. In fact, this proposed modification would seem to render the combined structure unsatisfactory for its intended purpose as a gate electrode stack by introducing a gate insulating layer between the conductive layers. Such a modification is prohibited under MPEP 2143.01.

Instead, the proposed modification appears to based on hindsight reconstruction wherein pieces of various references are picked, while ignoring other parts of the references, to arrive at the claimed invention (using the claims as a blue-print to do so). This is improper, and the rejection based thereon should be withdrawn.

Accordingly, it is respectfully requested that this rejection be withdrawn.

Information Disclosure Statement

Applicants are enclosing herewith an Information Disclosure Statement (IDS). It is respectfully requested that this IDS be entered and considered prior to the issuance of any further action for this application.

Conclusion

For at least the above-stated reasons, the claims of the present application are patentable over the cited references and should be allowed.

If the Examiner disagrees with Applicants or has any further rejections, it is requested that she call the undersigned to discuss.

If any further fee should be due for this amendment, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Date: December 3, 2004

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Registration No. 34,225

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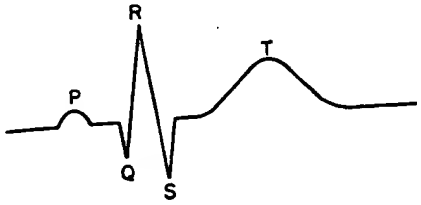
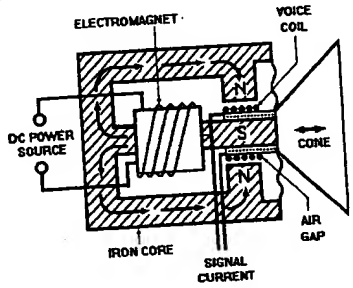
electric shock *Shock.*
electric strength *Dielectric strength.*
electric vector *Electric field vector.*
electroacoustic The operation of a product or device based on both electricity and acoustics, such as a loudspeaker or microphone.
electroacoustic effect *Acoustoelectric effect.*
electroacoustic transducer A transducer that receives waves from an electric system and delivers waves to an acoustic system, or vice versa.
electrocardiogram [ECG or EKG] A record made by an electrocardiograph. It is also called a cardiogram.



Electrocardiogram showing a typical tracing with electrodes on the surface of body. The initial P wave, produced by electric activation of atrium, is about 90 ms in duration. The peaked QRS complex due to activation of the ventricles lasts about 80 ms. The final slowly varying T wave is related to electric recovery of the ventricles.

electrocardiograph [ECG or EKG] An instrument for recording the waveforms of voltages developed in the chest and lower parts of the human body in synchronism with the action of the heart.
electrochemical machining A metal-cutting process that is the reverse of electroplating. A low DC voltage is applied between the workpiece and a tool having the shape of the desired cut, and an electrolyte is pumped at high pressure through the gap between workpiece and tool. Electrochemical action in the gap erodes metal from the workpiece.
electrode 1. A conducting element that performs one or more of the functions of emitting, collecting, or controlling the movements of electrons or ions in an electron tube, or the movements of electrons or holes in a semiconductor device. 2. A terminal or surface at which electricity passes from one material or medium to another, as at the electrodes of a battery, electrolytic capacitor, or weider. 3. One of the terminals used in dielectric heating or diathermy for applying the high-frequency electric field to the material being heated.
electrodeless discharge A luminous discharge produced by a high-frequency electric field in a gas-filled glass tube with no internal electrodes.
electrodeposition The process of depositing a substance on an electrode by electroplating or electroforming. It is also called electrolytic deposition.
electrode potential 1. The instantaneous voltage of an electrode with respect to the cathode of an electron tube. 2. The voltage existing between an electrode and the solution or electrolyte in which it is immersed.
electrode radiator A metal structure, often with a large area, that is an external extension of an electrode of an electron tube to facilitate the dissipation of heat. See *heatsink.*
electrodermal reaction The change in electric resistance of the skin during emotional stress. This is one of the functional variables measured by polygraphs.
electrodesiccation The destruction of tissue by electric sparks generated at the tip of a small movable electrode.
electrode voltage The voltage between an electrode and the cathode or a specified point on a filamentary cathode of an electron tube.
electrodiagnosis Diagnosis of disease by studying electric activity of parts of the body and responses to stimulation of electrically excitable tissues.
electrodynamic instrument An instrument that depends for its operation on the reaction between the current in one or more movable coils and the current in one or more fixed coils.

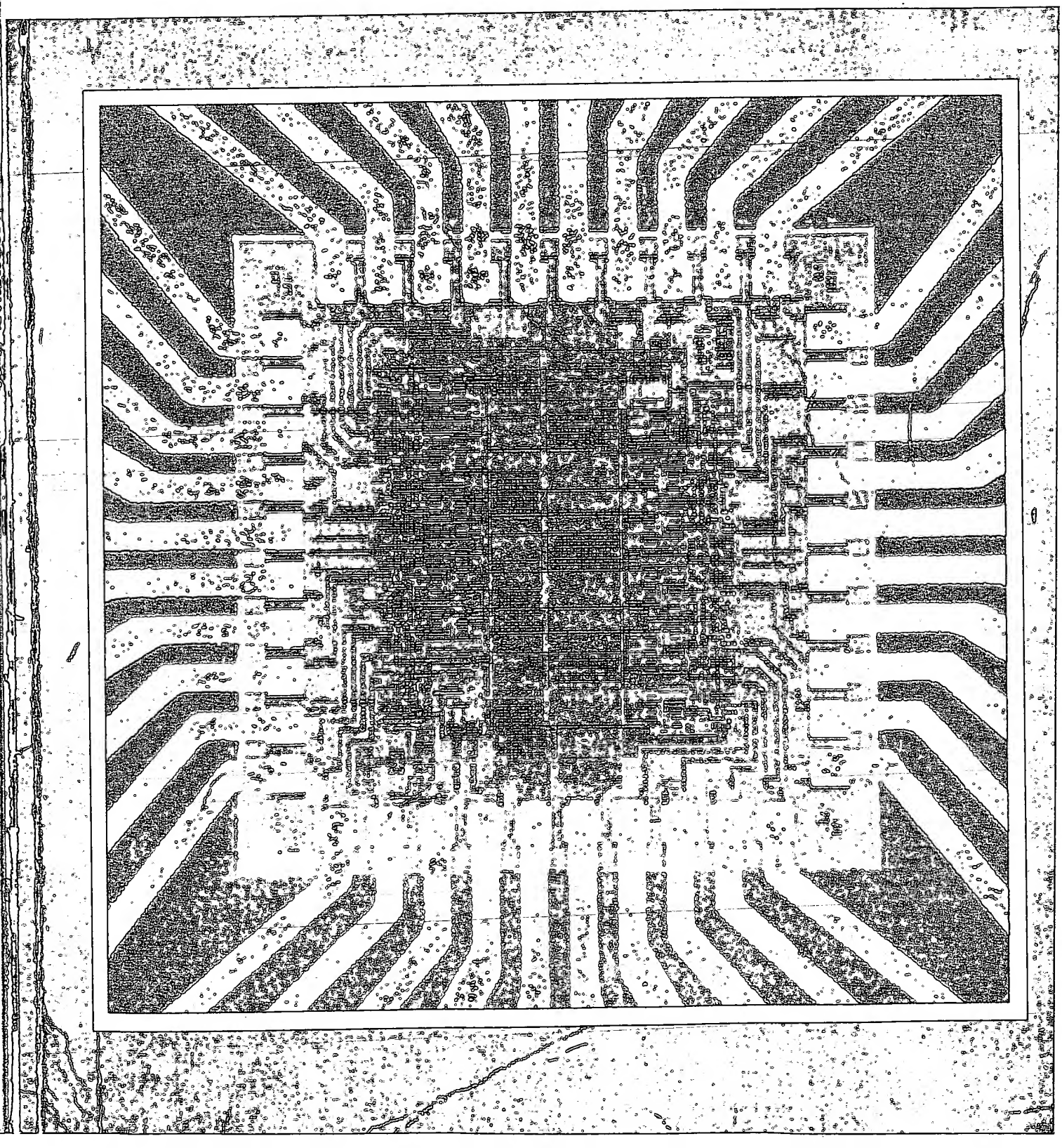


Electrodynamic speaker operation depends on the interaction between the electromagnet and the voice coil.

electrodynamic loudspeaker *Excited-field loudspeaker.*
electrodynamometer A low-frequency, transmission-type power meter that is connected between a source and a load. The current-sensing element is a fixed or stationary coil, and the voltage-sensing element is a movable or potential coil which rotates in the magnetic field of the stationary coil. The torque on the movable coil is opposed by a spring and is proportional to the average value of the instantaneous product of the currents in the two coils. The load current passes through the current-coil terminals, and the voltage terminals are connected across the load. The current through the movable coil is proportional to the load voltage, so its angular rotation is a function of the instantaneous voltage-current product. The pointer then indicates the average load power.
electroflor A material that changes color when electrically activated but does not radiate light.
electrofluiddynamic converter A converter that transforms the dynamic energy of a gaseous fluid into electric energy by passing through an electrostatic field a gas which contains electrically charged particles. The action is similar to that of a Van de Graaff generator, but higher power density can be obtained.
electroforming 1. The electrodeposition of metal on a conducting mold in sufficient thickness to make a desired metal object, such as a complex waveguide structure. The mold is often of graphite-coated wax so it can be removed by melting. 2. Production of a PN junction in a point-contact diode or transmitter by passing a large current pulse through the semiconductor material.

A SCIENTIFIC AMERICAN Book

MICROELECTRONICS



The Cover

The photograph on the cover symbolizes the theme of this issue of SCIENTIFIC AMERICAN: microelectronics, the art of putting complex electronic circuits on "chips" of silicon roughly a quarter of an inch square. The blue area in the center of the photograph is a single chip, a high-speed current-mode logic integrated circuit made by Texas Instruments Incorporated for a Honeywell Information Systems computer. Arrayed around the chip are 40 leads that connect it with its external environment. The leads are made of tin-plated copper. They are connected by an automatic process in which they are bonded by heat and compression to gold bumps plated at edge of the chip. The photograph was made by Fritz Goro in the Laboratory for Applied Microscopy of E. Leitz, Inc.

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CONTENTS

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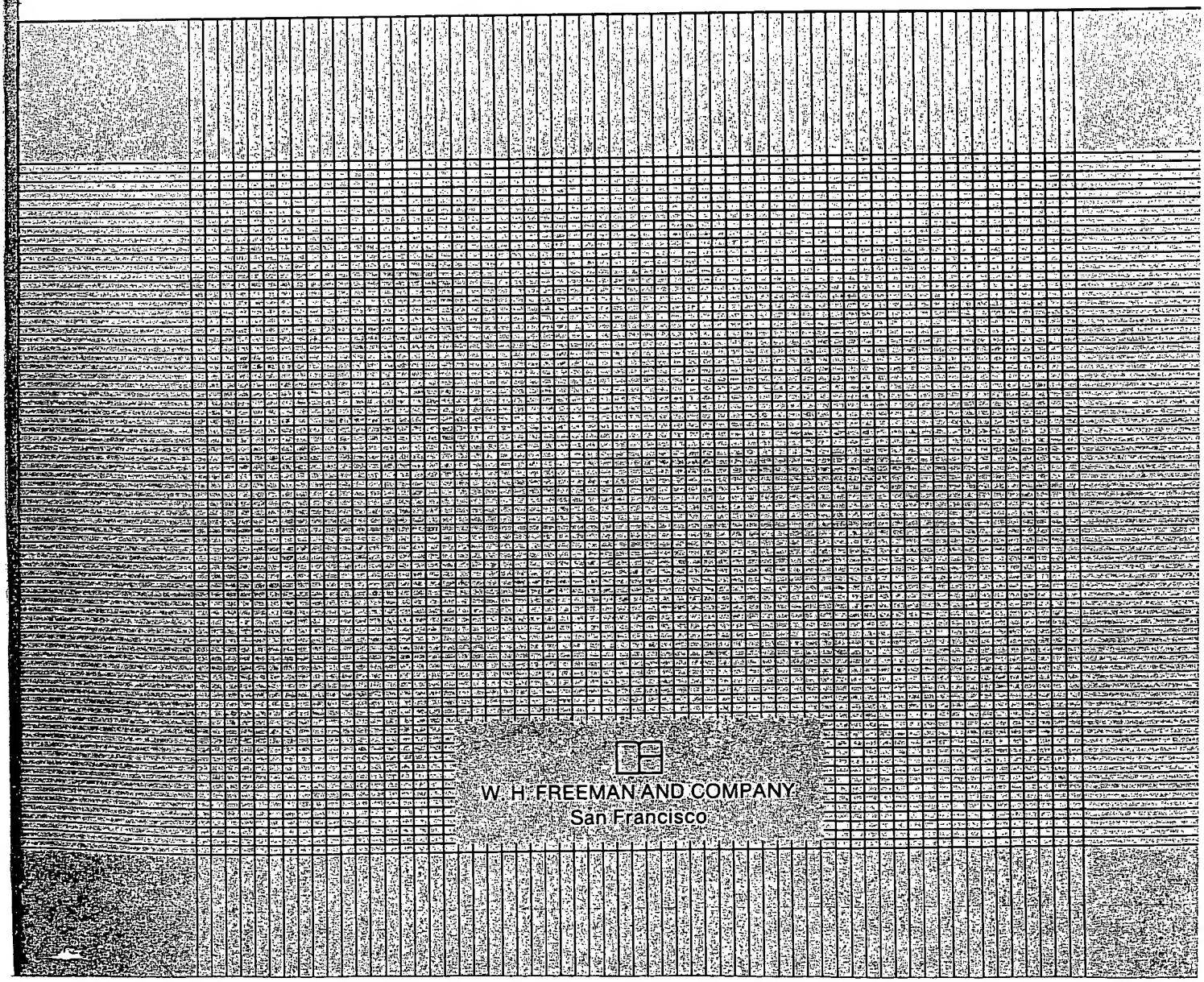
MICROELECTRONICS



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trolling the depth to which impurities diffuse are time and temperature. For example, a layer of phosphorus one micrometer deep can be diffused in about an hour at 1,100 degrees.

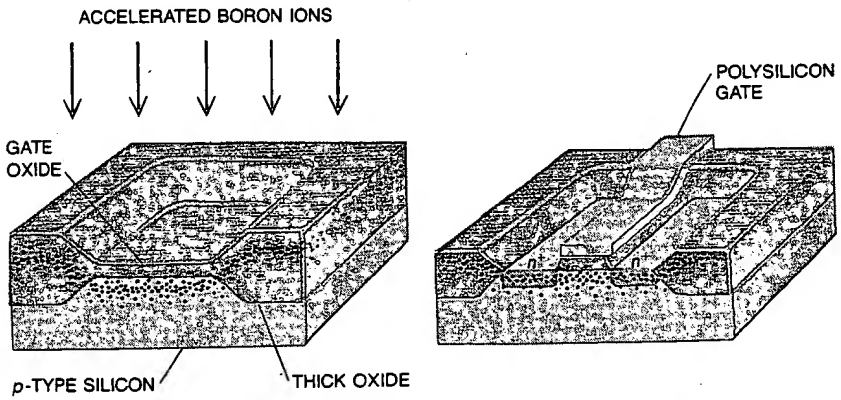
To achieve maximum control most diffusions are performed in two steps. The predeposit, or first, step takes place in a furnace whose temperature is selected to achieve the best control of the amount of impurity introduced. The temperature determines the solubility of the dopant in the silicon, just as the temperature of warm water determines the solubility of an impurity such as salt. After a comparatively short predeposit treatment the wafer is placed in a second furnace, usually at a higher temperature. This second heat treatment, the "diffusion drive-in" step, is selected to achieve the desired depth of diffusion.

In the formation of *pn* junctions by solid-state diffusion the impurities diffuse laterally under the oxide mask about the same distance as the depth of the junction. The edge of the *pn* junction is therefore protected by a layer of silicon dioxide. This is an important feature of the technique, because silicon dioxide is a nearly ideal insulator, and many of the electronic devices will not tolerate any leakage at the edge of the junction.

Another selective doping process, ion implantation, has been developed as a means of introducing impurities at room temperature. The dopant atoms are ionized (stripped of one or more of their electrons) and are accelerated to a high energy by passing them through a potential difference of tens of thousands of volts. At the end of their path they strike the silicon wafer and are embedded at various depths depending on their mass and their energy. The wafer can be selectively masked against the ions either by a patterned oxide layer, as in conventional diffusion, or by a photoresist pattern. For example, phosphorus ions accelerated through a potential of 100,000 volts will penetrate the photoresist to a depth of less than half a micrometer. Wherever they strike bare silicon they penetrate to an average depth of a tenth of a micrometer. Thus even a one-micrometer layer of photoresist can serve as a mask for the selective implantation of phosphorus.

As the accelerated ions plow their way into the silicon crystal they cause considerable damage to the crystal lattice. It is possible to heal most of the damage, however, by annealing the crystal at a moderate temperature. Little diffusion takes place at the annealing temperature, so that the ion-implantation conditions can be chosen to obtain the desired distribution. For example, a very shallow, high concentration of dopant can be conveniently achieved by ion implantation. A more significant feature of the technique is the possibility of accurately controlling the concentration of the dopant. The ions bombarding the crystal each carry a charge, and by measuring the total charge that accumulates the number of impurities can be precisely determined. Hence ion implantation is used whenever the doping level must be very accurately controlled. Often ion implantation simply replaces the predeposit step of a diffusion process. Ion implantation is also used to introduce impurities that are difficult to predeposit from a high-temperature vapor. For example, the current exploration of the use of arsenic as a shallow *n*-type dopant in MOS devices coincides with the availability of suitable ion-implantation equipment.

A unique feature of ion implantation is its ability to introduce impurities through a thin oxide. This technique is particularly advantageous in adjusting the threshold voltage of MOS transistors. Either *n*-type or *p*-type dopants can be implanted through the gate oxide, resulting in either a decrease or an increase of the threshold voltage of the device. Thus by means of the ion-implantation technique it is possible to fabricate several different types of MOS transistors on the same wafer.



ION IMPLANTATION is employed to place a precisely controlled amount of dopant (in this case boron ions) below the gate oxide of an MOS transistor. By choosing a suitable acceleration voltage the ions can be made to just penetrate the gate oxide but not the thicker oxide (*left*). After the boron ions are implanted polycrystalline silicon is deposited and patterned to form the gate regions of the transistor. A thin layer of the oxide is then removed, and the source and drain regions of the transistor are formed by the diffusion of an *n*-type impurity (*right*).

The uppermost layers of integrated circuits are formed by depositing and patterning thin films. The two most important processes for the deposition of thin films are chemical-vapor deposition and evaporation. The polycrystalline silicon film in the important silicon gate MOS technology is usually laid down by means of chemical-vapor deposition. Silane gas (SiH_4) decomposes when it is heated, releasing silicon and hydrogen. Accordingly when the wafers are heated in a dilute atmosphere of silane, a uniform film of polycrystalline silicon slowly forms on the surface. In subsequent steps the film is doped, oxidized and patterned.

It is also possible to deposit insulating films such as silicon dioxide or silicon nitride by means of chemical-vapor deposition. If a source of oxygen such as carbon dioxide is present during the decomposition of silane, silicon dioxide is formed. Similarly, silicon nitride is grown by decomposing silane in the presence of a nitrogen compound such as ammonia.

Evaporation is perhaps the simplest method of all for depositing a thin film and it is commonly employed to lay down the metallic conducting layer in most integrated circuits. The metal charge to be evaporated, usually aluminum, is placed in a crucible, and the wafers to be coated are placed above the crucible in a movable fixture called a planetary. During evaporation the wafers are rotated in order to ensure the maximum uniformity of the layer. The motion of the planetary also wobbles the wafers with respect to the source in order to obtain a continuous aluminum film over the steps and bumps on the surface created by the preceding photolithographic steps. After a glass bell jar is lowered over the planetary device and a high vacuum is established the aluminum charge is heated by direct bombardment with high-energy electrons. A pure aluminum film, typically about a micrometer thick, is deposited on the wafer.

In the fabrication of a typical large scale integrated circuit there are more thin-film steps than diffusion steps. Therefore thin-film technology is probably more critical to the overall yield and performance of the circuits than the diffusion and oxidation steps are. In a recent development a thin film is even employed to select the areas on a wafer that are to be oxidized. The compound silicon nitride has the property that it oxidizes much more slowly than silicon. A layer of silicon nitride can be vapor deposited, patterned and used as an oxidation mask. The surface that results